Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **D1**
2. **D0**
3. **VRB**
4. **AGND**
5. **VCCA**
6. **VIN**
7. **VRT**
8. **O/UF**
9. **D7**
10. **D6**
11. **D5**
12. **D4**
13. **CLK**
14. **DGND**
15. **VCCD**
16. **VCC01**
17. **OGND**
18. **VSS02**
19. **OE**
20. **D3**
21. **D2**

**.134”**

**2 1 21 20 19**

**18**

**17**

**16**

**15**

**14**

**13**

**3**

**4**

**5**

**6**

**7**

**8 9 10 11 12**

**5143K**

**MASK**

**REF**

**.134”**

**Top Material: Al/Si/Cu**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND (Powered Up)**

**Mask Ref: 51434K**

**APPROVED BY: DK DIE SIZE .134” X .134” DATE: 8/25/21**

**MFG: HARRIS THICKNESS .019” P/N: HI5714**

**DG 10.1.2**

#### Rev B, 7/1